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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,899	06/29/2005	Motoo Asai	259189US90PCT	2986

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EXAMINER	
JAHAN, BILKIS	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
04/10/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/509,899	ASAI ET AL.	
	Examiner	Art Unit	
	BILKIS JAHAN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) *12-71* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 6,-8, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt et al (5,822,856) in view of Kanber (5,312,765).

Regarding claim 1, Bhatt et al discloses a substrate (Fig. 5) for mounting an IC chip 614 (Fig. 6 col. 9, lines 38-43) comprising:

- an insulating substrate 302 (Fig. 4, col. 3, lines 55-65, Fig. 5, space between elements 504, 506) having a first surface 504, 530, 532 (Fig. 5) and a second surface 506, 534, 536 (Fig. 5) on an opposite side of the first surface (Fig. 5);
- a first built-up structure 537 (Fig. 5, col. 8, line 41) formed on the first surface of the insulating substrate 302 and comprising a conductor circuit 614 (Fig. 6 col. 9, lines 38-43) and an interlaminar insulating layer 508 (Fig. 5, col. 7, line 37, col. 8, lines 35-36);
- a second built-up structure 536 (Fig. 5, col. 8, line 39) formed on the second surface of the insulating substrate (Fig. 5, between elements 504, 506) and

comprising a conductor circuit 624 (Fig. 6, col. 9, line 41) and an interlaminar insulating layer 510 (Fig. 5, col. 7, line 37, col. 8, lines 35-36);

- a solder resist layer 533 (Fig. 5, col. 8, line 28) formed as an outermost layer over the first built-up structure 537;
- an element 614 mounted over the solder resist layer 533; and a path (Fig. 5, between elements 518, 538) for transmitting signal to or from the element 614 and penetrating through the insulating substrate (Fig. 5, space between elements 504, 506), first built-up structure 537, second built-up structure 536 and solder resist layer 533.
- Bhatt does not explicitly disclose the element is an **optical** element; the path is an **optical** path for transmitting optical signal to or from the **optical** element.
- However, Kanber discloses the element is an **optical** element 76, 84 (Fig. 12, col. 6, lines 21-22, col. 3, lines 49-50); the path is an **optical** path 92 (Fig. 12, col. 6, lines 38-41) for transmitting optical signal 94 to or from the **optical** element 76, 84. Kanber teaches the above modification is used to improve the heat dissipation efficiency and make strong substrate (col. 2, lines 38-41) and obtain low power consumption of the device (col. 1, lines 48-51). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Bhatt's structure with Kanber's structure as suggested above to improve the heat dissipation efficiency and make strong substrate (col. 2, lines 38-41) and obtain low power consumption of the device (col. 1, lines 48-51).

Regarding claim 2, Bhatt et al modified by Kanber discloses said optical path for transmitting optical signal comprises a vacancy (Kanber, col. 6, lines 38-41).

Regarding claim 6, Bhatt et al in view of Kanber discloses all limitations in claim 1 above.

Regarding claim 7, Bhatt et al modified by Kanber disclose said optical element is at least one of a light receiving element and a light emitting element (Kanber, col. 3, lines 49-50).

Regarding claim 8, Bhatt et al further disclose an electronic component 614 mounted on a surface of one of the solder resist layer 533.

Regarding claim 10, Bhatt et al modified by Kanber discloses some limiations in claim 1 above but do not disclose the optical path for transmitting optical signal has a cross-sectional diameter which is 100 to 500 nm.

- However, it would have been obvious to one of ordinary skill in the art to use any suitable diameter for the device, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Alner, 220 F .2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 11, Bhatt further discloses the hole 518, 538 connecting the conductor circuit 614 of the first built-up structure 537 and the conductor circuit 624 of the second built-up structure 536 through the insulating substrate 302 and via-hole 518, 538 connecting the conductor circuit 614 in the first built-up structure 537 and another conductor circuit 612 (Fig. 6) in the first-built-up structure 537 through the interlaminar insulating layer 508 in the first built-up structure 537.

Claims 3, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt et al (5,822,856), Kanber (5,312,765) and further in view of Lee et al (5,452,283).

Regarding claim 3, Takeuchi et al modified by Kanber disclose limitations above but do not disclose said optical path for transmitting optical signal comprises a resin composition.

- However, Lee et al disclose said optical path for transmitting optical signal is constituted by a resin composition 76 (Fig. 6, col. 5, lines 27-30). Lee teaches resin in the optical path is used to align the optical path to the objective lenses of the disk array (col. 2, lines 43-46). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Bhatt's structure with Lee's structure including resin to align the optical path to the objective lenses of the disk array (col. 2, lines 43-46).

Regarding claim 9, Bhatt et al modified by Kanber and Lee et al disclose a micro lens 30 (Lee, Fig. 7, col. 5, lines 53-58) disposed on an end portion of the optical path for transmitting optical signal (Lee, Fig. 7).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt et al (5,822,856), Kanber (5,312,765) and further in view of Stone (5,530,288).

Regarding claim 4, Bhatt et al modified by Kanber disclose limitations above but do not disclose said optical path for transmitting optical signal comprises a vacancy and a conductor layer around the vacancy.

- However, Stone discloses said optical path for transmitting optical signal comprises a vacancy and a conductor layer around the vacancy 29 (Fig. 2, col. 7, lines45-50). Stone teaches conductive layer is used to connect from passive electronic components to the substrate and both sides of substrate component (col. 4, lines 63-67). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Bhatt's structure with Stone's structure including conductive layer to connect from passive electronic components to the substrate and both sides of substrate components (col. 4, lines 63-67).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt et al (5,822,856), Kanber (5,312,765) and further in view of Lee et al (5,452,283) and Stone (5,530,288).

Regarding claim 5, Bhatt et al modified by Kanber, Lee, and Stone disclose all limitations in claims 1-4 above.

Response to Arguments

Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BILKIS JAHAN whose telephone number is (571)270-5022. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

BJ